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FIG ...
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1 **Application of speaker modification techniques to phonetic vocoding**
Ribeiro, C.M.; Trancoso, I.M.;
Spoken Language, 1996. ICSLP 96. Proceedings., Fourth International Conference
on , Volume: 1 , 3-6 Oct. 1996
Pages:306 - 309 vol.1

[Abstract]   [PDF Full-Text (320 KB)]   **IEEE CNF**

2 **A pipelined gray code-to-natural binary decoder for use in a Josephson A/D
converter**
Spargo, J.; Jewett, R.; Van Duzer, T.;
Magnetics, IEEE Transactions on , Volume: 19 , Issue: 3 , May 1983
Pages:1255 - 1258

[Abstract]   [PDF Full-Text (600 KB)]   **IEEE JNL**

3 **Design of fixed-point iterative decoders for concatenated codes with interleavers**
Montorsi, G.; Benedetto, S.;
Selected Areas in Communications, IEEE Journal on , Volume: 19 , Issue: 5 , May 2001
Pages:871 - 882

[Abstract]   [PDF Full-Text (380 KB)]   **IEEE JNL**

4 **Design of fixed-point iterative decoders for concatenated codes with interleavers**
Montorsi, G.; Benedetto, S.;
Global Telecommunications Conference, 2000. GLOBECOM '00. IEEE , Volume: 2 , 27 Nov.-1
Dec. 2000
Pages:801 - 806 vol.2

[Abstract]   [PDF Full-Text (724 KB)]   **IEEE CNF**

5 **Compiler-driven cached code compression schemes for embedded ILP processors**
Larin, S.Y.; Conte, T.M.;
Microarchitecture, 1999. MICRO-32. Proceedings. 32nd Annual International Symposium
on , 16-18 Nov. 1999

Pages:82 - 92

[Abstract]   [PDF Full-Text (120 KB)]   **IEEE CNF**

6 **A new multiple path search technique for residual vector quantizers**
Barnes, C.F.;
Data Compression Conference, 1994. DCC '94. Proceedings , 29-31 March 1994
Pages:42 - 51

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1 Special session on reconfigurable computing: Reconfigurable platforms for ubiquitous computing ▩

Manfred Glesner, Thomas Hollstein, Leandro Soares Indrusiak, Peter Zipf, Thilo Pionteck, Mihail Petrov, Heiko Zimmer, Tudor Murgan

April 2004　　**Proceedings of the first conference on computing frontiers on Computing frontiers**

Full text available: 📄 pdf(479.27 KB)　　Additional Information: full citation, abstract, references, index terms.

Ubiquitous computing requires flexibilty. Melting distributed electronic devices into everyday's life implies the need to adapt to evolving standards and dynamic environments. Furthermore, to gain user acceptance, such devices should be able to adapt to different usage patterns and user profiles. Scalability is also an important issue, allowing functional enhancements to already deployed systems. In this work we address these issues applying the concept of reconfigurability on different abstract ...

Keywords: communication, dynamic power management, networks-on-chip, reconfigurable hardware, reconfigurable processors, reconfiguration, ubiquitous computing

2 System partitioning and timing analysis: Design of multi-tasking coprocessor control for Eclipse ▩

Martijn J. Rutten, Jos T. J. van Eijndhoven, Evert-Jan D. Pol

May 2002　　**Proceedings of the tenth international symposium on Hardware/software codesign**

Full text available: 📄 pdf(846.07 KB)　　Additional Information: full citation, abstract, references, citings, index terms.

Eclipse defines a heterogeneous multiprocessor architecture template for data-dependent stream processing. Intended as a scalable and flexible subsystem of forthcoming media-processing systems-on-a-chip, Eclipse combines application configuration flexibility with the efficiency of function-specific hardware, or coprocessors. To facilitate reuse, Eclipse separates coprocessor *functionality* from generic support that addresses multi-tasking, inter-task synchronization, and data transport. Fi ...

3 Hardware/software partitioning for multi-function systems ▩

Asawaree Kalavade, P. A. Subrahmanyam

November 1997　**Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available: 📄 pdf(05.56 KB) 📄 Publisher Site.　　Additional Information: full citation, abstract, references, citings, index terms.

We are interested in optimizing the design of multi-function embedded systems that run a pre-specified set of applications, such as multi-standard audio/video codecs and multi-system phones. Such systems usually have stringent performance constraints and tend to have mixed hardware-software implementations. The current state of the art in the hardware/software codesign of such systems is to design for each application separately. This often leads to application-specific sub-optimal decisions and ...

Keywords: multi-function systems, hardware-software codesign, hardware/software partitioning, system-level design, core-based design, video encode/decode

4 Dedicated circuits: A multi-standard channel-decoder for base-station applications ☐

Timo Vogt, Norbert Wehn, Philippe Alves

September 2004　**Proceedings of the 17th symposium on Integrated circuits and system design**

Full text available: pdf(119.43 KB)   Additional Information: full citation, abstract, references, index terms

In this paper, a VLSI implementation of a multi-standard channel-decoder for EDGE, WCDMA, and CDMA2k convolutional-codes is presented. The new architecture employs the MAP algorithm for convolutional decoding to support soft-outputs.The decoder is designed for base-station applications. The maximum throughput of the decoder is 16 Mbps for WCDMA and CDMA2k, and 70 Mbps for EDGE, at a clock frequency of 200 MHz.

Keywords: CDMA2k, MAP, W-CDMA, configurable, convolutional decoder, hardware sharing, wireless

5 VLSI Design: On the high-speed VLSI implementation of errors-and-erasures correcting reed-solomon decoders
Tong Zhang, Keshab K. Parhi
April 2002   **Proceedings of the 12th ACM Great Lakes symposium on VLSI**

Full text available: pdf(149.39 KB)   Additional Information: full citation, abstract, references, index terms

Recently a novel algorithm transformation was proposed to reduce the critical path of Berlekamp-Massey algorithm implementation for errors-alone Reed-Solomon decoding. In this paper, we apply the same methodology to transform the Berlekamp-Massey algorithm for errors-and-erasures RS decoding. We present a regular hardware architecture to implement the reformulated Berlekamp-Massey algorithm, which can achieve high throughput. Moreover, an operation scheduling scheme is proposed to further reduce ...

Keywords: Berlekamp-Massey algorithm, Reed-Solomon codes, VLSI architectures, erasure

6 Design of low-power high-speed maximum a priori decoder architectures
A. Worm, H. Lamm, N. Wehn
March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(129.21 KB)   Additional Information: full citation, references, citings, index terms

7 Case studies in embedded system design: Design of a high-throughput low-power IS95 Viterbi decoder
Xun Liu, Marios C. Papaefthymiou
June 2002   **Proceedings of the 39th conference on Design automation**

Full text available: pdf(203.92 KB)   •   Additional Information: full citation, abstract, references, index terms

The design of high-throughput large-state Viterbi decoders relies on the use of multiple arithmetic units. The global communication channels among these parallel processors often consist of long interconnect wires, resulting in large area and high power consumption. In this paper, we propose a data-transfer oriented design methodology to implement a low-power 256-state rate-1/3 IS95 Viterbi decoder. Our architectural level scheme uses operation partitioning, packing, and scheduling to analyze an ...

Keywords: bus reduction, communications, pipelining

8 A 50 Mbit/s iterative turbo-decoder
F. Viglione, G. Masera, G. Piccinini, M. Ruo Roch, M. Zamboni
January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available:
pdf(69.06 KB)   Additional Information: full citation, references, citings, index terms
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9 Case studies: A low-cost and low-power multi-standard video encoder
R. Peset Llopis, R. Sethuraman, C. Alba Pinto, H. Peters, S. Maul, M. Oosterhuis
October 2003 **Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**
Full text available: pdf(541.20 KB)   Additional Information: full citation, abstract, references, index terms

Video encoders are an important IP block in mobile multimedia systems. In this paper, we describe a low-cost low-power multi-standard (MPEG4, JPEG, and H.263) video/image encoder. The low-cost and low-power aspects are achieved by the right choice of algorithms and architectures. In the algorithm front, an

embedded compression technique for reducing the size of loop memory has enabled a single-chip low-cost realization of the encoder. In the architectural front, an efficient hardware-software pa ...

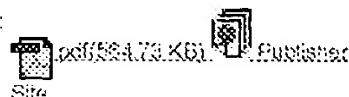**Keywords:** ASIPs, hardware/software partitioning, low-cost, low-power, multi-standard, video encoder

[10] Architecture Implementation Using the Machine Description Language LISA
Oliver Schliebusch, Andreas Hoffmann, Achim Nohl, Gunnar Braun, Heinrich Meyr
January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available:
pdf(584.73 KB) Publisher Site   Additional Information: full citation, abstract

The development of application specific instruction set processors comprises several design phases: architecture exploration, software tools design, system verification and design implementation. The LISA processor design platform LPDP based on machine descriptions in the LISA language provides one common environment for these design phases. Required software tools for architecture exploration and application development can be generated from one sole specification. This paper focuses on the imp ...

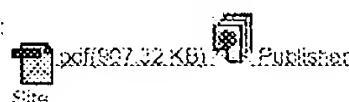**Keywords:** ASIP, Exploration, Implementation, Design, Synthesis, VHDL, Verilog, SystemC, LISA

[11] Register file and memory system design: Dynamic addressing memory arrays with physical locality
Steven Hsu, Shih-Lien Lu, Shih-Chang Lai, Ram Krishnamurthy, Konrad Lai
November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**

Full text available:
pdf(907.32 KB) Publisher Site   Additional Information: full citation, abstract, references, index terms

As pipeline width and depth grow to improve performance, memory arrays in microprocessors are growing in entries and ports. Arrays will increase in physical size, which prolongs the access time due to wiring delay. In order to boost clock frequency, these memory arrays must take multiple cycles to complete an access. This delays the scheduling of dependent instructions and affects overall performance. This paper proposes a different circuit organization to enable fast and slow accesses solely de ...
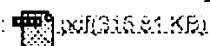
[12] Power- and Energy-Aware Computing: Comparing power consumption of an SMT and a CMP DSP for mobile phone workloads
Stefanos Kaxiras, Girija Narlikar, Alan D. Berenbaum, Zhigang Hu
November 2001 **Proceedings of the international conference on Compilers, architecture, and synthesis for embedded systems**

Full text available: pdf(316.51 KB)   Additional Information: full citation, abstract, references, citings, index terms

In the DSP world, many media workloads have to perform a specific amount of work in a specific period of time. This observation led us to examine Simultaneous Multithreading (SMT) and Chip Multiprocessing (CMP) for a VLIW DSP architecture (specifically the Star*Core SC140), in conjunction with Frequency/Voltage scaling to decrease dynamic power consumption in next-generation wireless handsets. We study the resulting performance and power characteristics of the two approaches using simulation, co ...
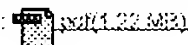
[13] Pipelined memory shared buffer for VLSI switches
Manolis Katevenis, Panagiota Vatsolaki, Aristides Efthymiou
October 1995 **ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Applications, technologies, architectures, and protocols for computer communication, Volume 25 Issue 4**

Full text available: pdf(1.22 MB)   Additional Information: full citation, abstract, references, citings, index terms

Switch chips are building blocks for computer and communication systems. Switches need internal buffering, because of output contention; shared buffering is known to perform better than multiple input queues or buffers, and the VLSI implementation of the former is *not* more expensive than the latter. We present a new organization for a shared buffer with its associated switching and cut-through functions. It is simpler and smaller than wide or interleaved organizations, and it is particula ...
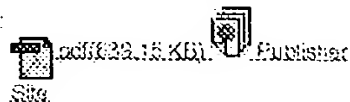
Keywords: crossbar switch, gigabit VLSI switch buffer, input queueing, multiport buffer, pipelined memory, shared buffering

[14] Instruction encoding techniques for area minimization of instruction ROM

T. Okuma, H. Tomiyama, A. Inoue, E. Fajar, H. Yasuura
December 1998 **Proceedings of the 11th international symposium on System synthesis**

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15 ~~Compiler-driven cached code compression schemes for embedded ILP processors~~
Sergei Y. Larin, Thomas M. Conte
November 1999 **Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture**
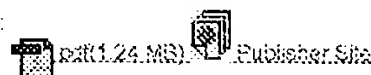
Full text available: ~~pdf(1.24 MB)~~ Publisher Site   Additional Information: full citation, abstract, references, citings, index terms

During the last 15 years, embedded systems have grown in complexity and performance to rival desktop systems. The architectures of these systems present unique challenges to processor microarchitecture, including instruction encoding and instruction fetch processes. This paper presents new techniques for reducing embedded system code size without reducing functionality. This approach is to extract the pipeline decoder logic for an embedded VLIW processor in software at system develo ...

16 ~~Banked multiported register files for high-frequency superscalar microprocessors~~
Jessica H. Tseng, Krste Asanović
May 2003   **ACM SIGARCH Computer Architecture News , Proceedings of the 30th annual international symposium on Computer architecture**, Volume 31 Issue 2
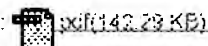
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Multiported register files are a critical component of high-performance superscalar microprocessors. Conventional multiported structures can consume significant power and die area. We examine the designs of banked multiported register files that employ multiple interleaved banks of fewer ported register cells to reduce power and area. Banked register files designs have been shown to provide sufficient bandwidth for a superscalar machine, but previous designs had complex control structures that w ...

17 ~~A DISE implementation of dynamic code decompression~~
Marc L. Corliss, E. Christopher Lewis, Amir Roth
June 2003   **ACM SIGPLAN Notices , Proceedings of the 2003 ACM SIGPLAN conference on Language, compiler, and tool for embedded systems**, Volume 38 Issue 7
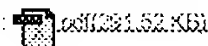
Full text available: ~~pdf(321.52 KB)~~   Additional Information: full citation, abstract, references, index terms

Code compression coupled with dynamic decompression is an important technique for both embedded and general-purpose microprocessors. *Post-fetch decompression*, in which decompression is performed after the compressed instructions have been fetched, allows the instruction cache to store compressed code but requires a highly efficient decompression implementation. We propose implementing post-fetch decompression using *dynamic instruction stream editing* (DISE), a programmable decoder-- ...

Keywords: DISE, code compression, code decompression

18 ~~Novel devices and approaches to programmable devices: Highly pipelined asynchronous FPGAs~~
John Teifel, Rajit Manohar
February 2004 **Proceeding of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**
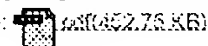
Full text available: ~~pdf(452.75 KB)~~   Additional Information: full citation, abstract, references, index terms

We present the design of a high-performance, highly pipelined asynchronous FPGA. We describe a very fine-grain pipelined logic block and routing interconnect architecture, and show how asynchronous logic can efficiently take advantage of this large amount of pipelining. Our FPGA, which does not use a clock to sequence computations, automatically self-pipelines" its logic without the designer needing to be explicitly aware of all pipelining details. This property makes our FPGA ideal for throughp ...

Keywords: asynchronous circuits, concurrency, correctness by construction, pipelining, programmable logic

19 ~~Allowing for ILP in an embedded Java processor~~
Ramesh Radhakrishnan, Deependra Talla, Lizy Kurian John
May 2000   **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2

Full text available: pdf(283.70 KB)   Additional Information: full citation, abstract, references, citings, index terms

Java processors are ideal for embedded and network computing applications such as Internet TV's, set-top boxes, smart phones, and other consumer electronics applications. In this paper, we investigate cost-effective microarchitectural techniques to exploit parallelism in Java bytecode streams. Firstly, we propose the use of a fill unit that stores decoded bytecodes into a decoded bytecode cache. This mechanism improves the fetch and decode bandwidth of Java processors by 2 to 3 time ...

20 Low power DSP's for wireless communications (embedded tutorial session)
Ingrid Verbauwhede, Chris Nicol
August 2000   **Proceedings of the 2000 international symposium on Low power electronics and design**

Full text available: pdf(424.32 KB)   Additional Information: full citation, abstract, references, citings, index terms

Wireless communications and more specifically, the fast growing penetration of cellular phones and cellular infrastructure are the major drivers for the development of new programmable Digital Signal Processors (DSPs). In this tutorial, an overview will be given of recent developments in DSP processor architectures, that makes them well suited to execute computationally intensive algorithms typically found in communications systems. DSP processors have adapted instruction sets, memory archi ...

Keywords: architectures, digital signal processing, programmable processors, wireless communications

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21 A 32-bit CMOS microprocessor with six-stage pipeline structure   ☐
H. Kaneko, Y. Miki, S. Nohara, K. Koya, M. Araki
November 1999 **Proceedings of 1986 ACM Fall joint computer conference**

Full text available: 📄 pdf(933.34 KB)   Additional Information: full citation, references, citings, index terms

22 Session 6C: Markovian analysis and asynchronous circuits: Pipeline optimization for asynchronous   ☐
circuits: complexity analysis and an efficient optimal algorithm
Sangyun Kim, Peter A. Beerel
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: 📄 pdf(113.08 KB)   Additional Information: full citation, abstract, references

This paper addresses the problem of identifying the minimal pipelining needed in an asynchronous circuit
(e.g., number/size of pipeline stages/latches required) to satisfy a given performance constraint, thereby
implicitly minimizing area and power for a given performance. In contrast to the somewhat analogous
problem of *retiming* in the synchronous domain, we first show that the basic pipeline optimization problem
for asynchronous circuits is NP-complete. This paper then presents an effic ...

23 Session 8: Floorplanning: Floorplanning of pipelined array modules using sequence pairs   ☐
Matthew Moe, Herman Schmit
April 2003   **Proceedings of the 2003 international symposium on Physical design**

Full text available: 📄 pdf(195.25 KB)   Additional Information: full citation, abstract, references, citings, index terms.

Floorplanning individual pipelined array modules of a larger overall die can yield beneficial results. Critical
paths in every pipeline stage of a pipelined design are roughly equivalent after synthesis. The inability of
synthesis tools to predict without full placement both wire congestion and the distance traveled by a wire or
wires between consecutive registers are the greatest causes of additional delay and area during place and
route. This paper will detail a floorplanning methodology for p ...

Keywords: floorplan, pipelined array, sequence pair

24 A reconfigurable multi-function computing cache architecture   ☐
Hue-Sung Kim, Arun K. Somani, Akhilesh Tyagi
February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field
                programmable gate arrays**

Full text available: 📄 pdf(982.08 KB)   Additional Information: full citation, abstract, references, citings, index terms.

A considerable portion of a chip is dedicated to a cache memory in a modern microprocessor chip. However,
some applications may not actively need all the cache storage, especially the computing bandwidth limited
applications. Instead, such applications may be able to use some additional computing resources. If the
unused portion of the cache could serve these computation needs, the on-chip resources would be utilized
more efficiently. This presents an opportunity to explore the reconfigurat ...

25   ☐
Real-time software-based video coder for multimedia communication systems

Ho Chao Huang, Jau-Hsiung Huang, Ja-Ling Wu
September 1993 **Proceedings of the first ACM international conference on Multimedia**

Full text available: pdf(119.90 KB) ps(190.26 KB)   Additional Information: full citation, references, index terms

Keywords: multimedia system, software-based video compression, video data compression, video phone/conference

26 The design of dynamically reconfigurable datapath coprocessors
Zhining Huang, Sharad Malik, Nahri Moreano, Guido Araujo
May 2004   **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 2

Full text available: pdf(457.62 KB)   Additional Information: full citation, abstract, references, index terms

Increasing nonrecurring engineering and mask costs are making it harder to turn to hardwired application specific integrated circuit (ASIC) solutions for high-performance applications. The volume required to amortize these high costs has been increasing, making it increasingly expensive to afford ASIC solutions for medium-volume products. This has led to designers seeking programmable solutions of varying sorts using these so-called programmable platforms. These programmable platforms span a lar ...

Keywords: Loop pipelining, coarse-grain reconfigurable fabric, datapath synthesis, interconnection design, reconfigurable datapath

27 Processors and accelerators for embedded applications: The iCOREtm 520 MHz synthesizable CPU core
Nick Richardson, Lun Bin Huang, Razak Hossain, Tommy Zounes, Naresh Soni, Julian Lewis
June 2002   **Proceedings of the 39th conference on Design automation**

Full text available: pdf(360.25 KB)   Additional Information: full citation, abstract, references, index terms

This paper describes a new implementation of the ST20-C2 CPU architecture. The design involves an eight-stage pipeline with hardware support to execute up to three instructions in a cycle. Branch prediction is based on a 2-bit predictor scheme with a 1024-entry Branch History Table and a 64 entry Branch Target Buffer and a 4-entry Return Stack. The implementation of all blocks in the processor was based on synthesized logic generation and automatic place and route. The full design of the CPU fro ...

Keywords: ASIC, CPU, branch-prediction, cache, embedded, high-frequency, microarchitecture, pipeline, st20, synthesis

28 A flexible VLSI core for an adaptable architecture
H. Mulder, P. Stravers
August 1989   **ACM SIGMICRO Newsletter , Proceedings of the 22nd annual workshop on Microprogramming and microarchitecture**, Volume 20 Issue 3

Full text available: pdf(846.24 KB)   Additional Information: full citation, abstract, references, citings, index terms

Two major limitations concerning the design of cost-effective application-specific architectures are the recurrent costs of system-software development and hardware implementation, in particular VLSI implementation, for each architecture. The SCalable ARChitecture Experiment (SCARCE) aims to provide a framework for application-specific processor design. The framework allows scaling of functionality, implementation complexity, and performance. The SCARCE framework consists and wil ...

29 Energy-driven integrated hardware-software optimizations using SimplePower
N. Vijaykrishnan, M. Kandemir, M. J. Irwin, H. S. Kim, W. Ye
May 2000   **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2

Full text available: pdf(314.70 KB)   Additional Information: full citation, abstract, references, citings, index terms

With the emergence of a plethora of embedded and portable applications, energy dissipation has joined throughput, area, and accuracy/precision as a major design constraint. Thus, designers must be concerned with both optimizing and estimating the energy consumption of circuits, architectures, and software. Most of the research in energy optimization and/or estimation has focused on single components of the system and has not looked across the interacting spectrum of the hardware and softwar ...

Keywords: compiler optimizations, energy optimization and estimation, energy simulator, hardware-software interaction, low-power architectures, system energy

30 A bipartition-codec architecture to reduce power in pipelined circuits
Shanq-Jang Ruan, Rung-Ji Shang, Feipei Lai, Shyh-Jong Chen, Xian-Jun Huang
November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(92.27 KB)　　　　Additional Information: full citation, abstract, references, index terms

This paper proposes a new bipatition-codec architecture that may reduce power consumption of pipelined circuits. We treat each output value of a pipelined circuit as one state of a FSM. If the output of a pipelined circuit transit mainly among few states, we could partition the combinational portion of a pipelined circuit into two blocks: one that contains the few states of high activity is small and the other that contains the remainder of low activity is big. Consequently, the state trans ...

31 Efficient instruction encoding for automatic instruction set design of configurable ASIPs
Jong-eun Lee, Kiyoung Choi, Nikil Dutt
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(356.80 KB)　　　　Additional Information: full citation, abstract, references, citings, index terms

Application-specific instructions can significantly improve the performance, energy, and code size of configurable processors. A common approach used in the design of such instructions is to convert application-specific operation patterns into new complex instructions. However, processors with a fixed instruction bitwidth cannot accommodate all the potentially interesting operation patterns, due to the limited code space afforded by the fixed instruction bitwidth. We present a novel instruction ...

32 An extended addressing mode for low power
Atul Kalambur, Mary Jane Irwin
August 1997 **Proceedings of the 1997 international symposium on Low power electronics and design**

Full text available: pdf(705.00 KB)　　　　Additional Information: full citation, references, citings

33 Achieving 550 MHz in an ASIC methodology
D. G. Chinnery, B. Nikolic, K. Keutzer
June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(1.21 MB)　　　　Additional Information: full citation, abstract, references, citings, index terms

Typically, good automated ASIC designs may be two to five times slower than handcrafted custom designs. At last year's DAC this was examined and causes of the speed gap between custom circuits and ASICs were identified. In particular, faster custom speeds are achieved by a combination of factors: good architecture with well-balanced pipelines; compact logic design; timing overhead minimization; careful floorplanning, partitioning and placement; dynamic logic; post-layout transistor and wire ...

Keywords: ASIC, clock, comparison, custom, frequency, speed, throughput

34 Improving CISC instruction decoding performance using a fill unit
Mark Smotherman, Manoj Franklin
December 1995 **Proceedings of the 28th annual international symposium on Microarchitecture**

Full text available: pdf(965.34 KB)　　　　Additional Information: full citation, references, citings, index terms

35 Sensitivity analysis of a superscalar processor model
Y. Zhu, W. F. Wong
January 2002 **Australian Computer Science Communications , Proceedings of the seventh Asia-Pacific conference on Computer systems architecture - Volume 6,** Volume 24 Issue 3

Full text available: pdf(826.31 KB)　　　　Additional Information: full citation, abstract, references, index terms

Superscalar processors obtain their performance by exploiting instruction level parallelism in programs. Their performance is therefore limited by characteristics of programs and the design of the processor. Due to the complexity involved, estimating the performance of any superscalar processor design is a difficult task. Quick prediction of performance improvement arising from architecture modifications is even more difficult. In this paper, a model of superscalar processors using a network of ...

Keywords: queuing theory, superscalar processors

36 High level power modeling and analysis: Microarchitectural power modeling techniques for deep sub-micron microprocessors
Nam Sung Kim, Taeho Kgil, Valeria Bertacco, Todd Austin, Trevor Mudge
August 2004   **Proceedings of the 2004 international symposium on Low power electronics and design**

Full text available: pdf(450.11 KB)   Additional Information: full citation, abstract, references, index terms

The need to perform early design studies that combine architectural simulation with power estimation has become critical as power has become a design constraint whose importance has moved to the fore. To satisfy this demand several microarchitectural power simulators have been developed around SimpleScalar, a widely used microarchitectural performance simulator. They have proven to be very useful at providing insights into power/performance trade-offs. However, they are neither parameterized nor ...

Keywords: deep sub-micron, power modeling

37 DISE: a programmable macro engine for customizing applications
Marc L. Corliss, E. Christopher Lewis, Amir Roth
May 2003   **ACM SIGARCH Computer Architecture News , Proceedings of the 30th annual international symposium on Computer architecture**, Volume 31 Issue 2

Full text available: pdf(336.30 KB)   Additional Information: full citation, abstract, references, citings

Dynamic Instruction Stream Editing (DISE) is a cooperative software-hardware scheme for efficiently adding customization functionality---e.g, safety/security checking, profiling, dynamic code decompression, and dynamic optimization---to an application. In DISE, application customization functions (ACFs) are formulated as rules for macro-expanding certain instructions into parameterized instruction sequences. The processor executes the rules on the fetched instructions, feeding the executi ...

38 Clock rate versus IPC: the end of the road for conventional microarchitectures
Vikas Agarwal, M. S. Hrishikesh, Stephen W. Keckler, Doug Burger
May 2000   **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2

Full text available: pdf(207.54 KB)   Additional Information: full citation, abstract, references, citings, index terms

The doubling of microprocessor performance every three years has been the result of two factors: more transistors per chip and superlinear scali ng of the processor clock with technology generation. Our results show that, due to both diminishing improvements in clock rates and poor wire scaling as semiconductor devices shrink, the achievable performance growth of conventional microarchitectures will slow substantially. In this paper, we describe technology-driven models for wire cap ...

39 Session 10B: Power saving techniques for embedded processors: A methodology for the design of application specific instruction set processors (ASIP) using the machine description language LISA
Andreas Hoffmann, Oliver Schliebusch, Achim Nohl, Gunnar Braun, Oliver Wahlen, Heinrich Meyr
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(913.02 KB)   Additional Information: full citation, abstract, references, citings, index terms

The development of application specific instruction set processors (ASIP) is currently the exclusive domain of the semiconductor houses and core vendors. This is due to the fact that building such an architecture is a difficult task that requires expertise knowledge in different domains: application software development tools, processor hardware implementation, and system integration and verification. This paper presents a retargetable framework for ASIP design which is based on machine descript ...

40 Trace cache: a low latency approach to high bandwidth instruction fetching
Eric Rotenberg, Steve Bennett, James E. Smith
December 1996 **Proceedings of the 29th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.33 MB) Publisher Site   Additional Information: full citation, abstract, references, citings, index terms

As the issue width of superscalar processors is increased, instruction fetch bandwidth requirements will also increase. It will become necessary to fetch multiple basic blocks per cycle. Conventional instruction caches hinder this effort because long instruction sequences are not always in contiguous cache locations. We propose supplementing the conventional instruction cache with a trace cache. This structure caches traces of the dynamic instruction stream, so instructions that are otherwise no ...

Keywords: instruction cache, instruction fetching, multiple branch prediction, superscalar processors, trace cache

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